WHAT IS CLAIMED IS:

1. A method for determining a high part of a floating point operand comprising:

determining a format of the floating point operand;

setting a plurality of exponent field digits and a plurality of fraction field digits of a result to a zero if the determined format is one of a first group comprising an infinity format and an overflow format;

setting the exponent field digits and the fraction field digits of the result to corresponding exponent field digits and corresponding fraction field digits of the floating point operand if the determined format is a not-a-number (NaN) format; and

adaptively clearing at least one of the fraction field digits of the result if the determined format is one of a second group comprising a denormalized format and a delimited format, wherein the high part of the floating point operand is the result.

2. The method of claim 1, wherein the determining step further comprises identifying the format based upon embedded status information within the floating point operand.

3. The method of claim 1, wherein the adaptively clearing step further comprises setting a low part of the fraction field digits of the result to one of two values if the determined format is the denormalized format, the two values being based upon the number of leading zeros in the fraction field digits of the floating point operand.

4. The method of claim 3, wherein the first of the two values is the corresponding low part of the fraction field digits of the floating point operand, and wherein the second of the two values is zero.

5. The method of claim 1, wherein the adaptively clearing step further comprises setting a low part of the fraction field digits of the result to one of two values if the determined format is the delimited format, the two values being based upon a delimiter flag.

6. The method of claim 5, wherein the first of the two values is the corresponding low part of the fraction field digits of the floating point operand, and wherein the second of the two values is zero.

7. The method of claim 5, wherein the delimiter flag is within the corresponding low part of the fraction field digits of the floating point operand.

8. The method of claim 5, wherein the adaptively clearing step comprises setting the corresponding low part of the fraction field digits to zero with the exception of the delimiter flag.

9. A computer-readable medium having instructions, which when executed perform a method for determining a high part of a floating point operand comprising:

determining a format of the floating point operand;

setting a plurality of exponent field digits and a plurality of fraction field digits of a result to a zero if the determined format is one of a first group comprising an infinity format and an overflow format;

setting the exponent field digits and the fraction field digits of the result to corresponding exponent field digits and corresponding fraction field digits of the floating point operand if the determined format is a not-a-number (NaN) format; and

adaptively clearing at least one of the fraction field digits of the result if the determined format is one of a second group comprising a denormalized format and a delimited format, wherein the high part of the floating point operand is the result.

10. The computer-readable medium of claim 9, wherein the determining step further comprises identifying the format based upon embedded status information within the floating point operand.

11. The computer-readable medium of claim 9, wherein the adaptively clearing step further comprises setting a low part of the fraction field digits of the result to one of two values if the determined format is the denormalized format, the two values being based upon the number of leading zeros in the fraction field digits of the floating point operand.

12. The computer-readable medium of claim 11, wherein the first of the two values is the corresponding low part of the fraction field digits of the floating point operand, and wherein the second of the two values is zero.

13. The computer-readable medium of claim 9, wherein the adaptively clearing step further comprises setting a low part of the fraction field digits of the result to one of two values if the determined format is the delimited format, the two values being based upon a delimiter flag.

14. The computer-readable medium of claim 13, wherein the first of the two values is the corresponding low part of the fraction field digits of the floating point operand, and wherein the second of the two values is zero.

15. The computer-readable medium of claim 13, wherein the delimiter flag is within the corresponding low part of the fraction field digits of the floating point operand.

16. The computer-readable medium of claim 13, wherein the adaptively clearing step comprises setting the corresponding low part of the fraction field digits to zero with the exception of the delimiter flag.

17. A system for determining a high part of a floating point operand, comprising:

an operand analysis circuit that determines a format associated with the floating point operand;

a processing circuit that adaptively sets at least one digit of an intermediate result; and

a result generator circuit that assembles a final result equal to the high part of the floating point operand based on the format of the floating point operand and the intermediate result.

18. The system of claim 17, wherein the operand analysis circuit determines the format based upon embedded status information within the floating point operand.

19. The system of claim 17, wherein the processing circuit is operative to adaptively set a low part of the fraction field digits of the intermediate result to one of two values if the determined format is a denormalized format, the two values being based upon the number of leading zeros in the fraction field digits of the floating point operand.

20. The system of claim 19, wherein the first of the two values is the corresponding low part of the fraction field digits of the floating point operand, and wherein the second of the two values is zero.

21. The system of claim 17, wherein the processing circuit is operative to adaptively set a low part of the fraction field digits of the intermediate result to one of two values if the determined format is a denormalized format, the two values being based upon a delimiter flag.

22. The system of claim 21, wherein the first of the two values is the corresponding low part of the fraction field digits of the floating point operand, and wherein the second of the two values is zero.

23. The system of claim 21, wherein the delimiter flag is within the corresponding low part of the fraction field digits of the floating point operand.

24. The system of claim 21, wherein processing circuit is further operative to set the corresponding low part of the fraction field digits to zero with the exception of the delimiter flag.